Summary of "Energy and Material Use in the Production of Semiconductor Devices"

Silicon microchips are the foundation of the modern information age. Computing devices rely on the capabilities of these micro-scale innovations to perform functions from storing information to performing complex calculations. However, despite their small size, microchip fabrication consumes extremely large amounts of energy and resources. Specifically, the mass of intermediate products used to produce a single microchip (including fossil fuels and various other chemicals involved in the purification and fabrication processes) amounts to 600 times the mass of the microchip itself. As an example, in the manufacture of automobiles, the intermediate products amount to only around twice as much as the mass of the vehicle. This mismatch can be attributed to the extremely ordered state of a silicon microchip, as these devices are the purest products manufactured at commercial scales. The manufacturing process thus involves moving from relatively high entropy reactants (mined quartz) to ultra-low entropy products (99.9999999% silicon wafers with precise patterning/machining), necessitating the consumption of huge amounts of energy [2]. In fact, producing wafer-quality silicon from raw silicon consumes 160 times as much energy as producing raw silicon from quartz. Humanity is already too dependent on the versatility and power provided by silicon microchip fabrication; however, we must keep in mind the environmental impacts of this dependence and strive to minimize consumption. To guide the development of more eco-friendly manufacturing methods, policies, and regulations, Williams, Ayres, and Heller compiled information from several organizations in "The 1.7 Kilogram Microchip: Energy and Material Use in the Production of Semiconductor Devices."

Williams, Ayres, and Heller use information from the Electronics Industry Association of Japan (EIAJ), the Toxics Release Inventory (TRI) program of the United States Environmental Protection Agency, and the United Nations Environment Program (UNEP) / United Nations Industrial Development Organizations (UNIDO) joint report to quantify energy and material use. Additionally, they feature figures from an anonymous firm for comparison and analysis purposes. However, these sources fail to quantify several inputs and outputs of the manufacturing process, particularly relating to materials consumed in wafer fabrication (as seen by the many chemical inputs excluded from analysis in Fig. 1 of [1]). This certainly limits the scope of the paper as a comprehensive overview; nevertheless, the striking numbers revealed despite this gap in information accomplish the goal of the authors in drawing attention to the issue. The proceeding sections break the manufacturing process down into steps of purification, fabrication, and packaging. An attempt is made to quantify the aggregate chemical use (in grams per square centimeter of wafer); however, the range of reported values is far too wide, spanning three orders of magnitude. The authors attribute the high variability to issues in agency data collection; particularly, the TRI data only measures chemical use at a firm if more than 11.3 metric tons are consumed. This may cause significant undercounting. Water consumption is then considered and found to be roughly 17 L per square cm of wafer.

Energy use is estimated from corroborating data from each of the organizations. Most of the data is direct; however, with regards to chemicals, the authors measure energy consumed in purifying the various chemicals for their use in silicon fabrication (since very high purities are needed, such as 99.999% semiconductor-grade ammonia). They arrive at the following figures for a 32 MB DRAM chip (using emissions and electricity consumption data): 5.8 MJ silicon purification chain, 2.3 MJ chemical production, 27 MJ fabrication, 5.8 MJ assembly process, 0.17 MJ assembly, and 15 MJ in product usage. This is per 1.6 square centimeters of input silicon. Overall, the main takeaway from the paper is that current energy and materials usage in semiconductor production is extremely high relative to the amount of semiconductor produced, and thus efforts should be put into more sustainable development. Additionally, current reporting/policies (particularly TRI) undercount the environmental impact of the semiconductor industry and should thus be re-evaluated.

Summary of Microfabrication Laboratory Project

Over the course of the semester, techniques of silicon microfabrication were employed to produce a microfluidic device (flow cytometer "on a chip"). Though functionally different from the semiconductor devices discussed in [1], the same methods and materials were used, and thus the same analysis is relevant to determine the environmental and economic impacts of developing the flow cytometer. First, a brief overview of the device. Flow cytometers quantify various characteristics of particles (usually cells) suspended in a bulk solution. Thus, they require techniques for collecting individual cell level measurements. The following device utlizes microchannels machined on a silicon wafer to focus a fluid stream for microscale measurements. Standard, four-inch silicon wafers (previously oxidized) were patterned with photolithography to produce a microchannel design capable of hydrodynamic focusing. This design was then etched into the wafer, followed by oxidation to electrically isolate the silicon. Thus, electrodes for electrokinetic focusing could be deposited on the surface of the wafer. Finally, the device was packaged via two different methods (anodic bonding of borosilicate glass and PDMS plasma bonding) for comparison purposes. A schematic of the device design and an image of the manufactured chip are included below in Fig. 1. The full production process is detailed in Fig. 2 (at end of document).

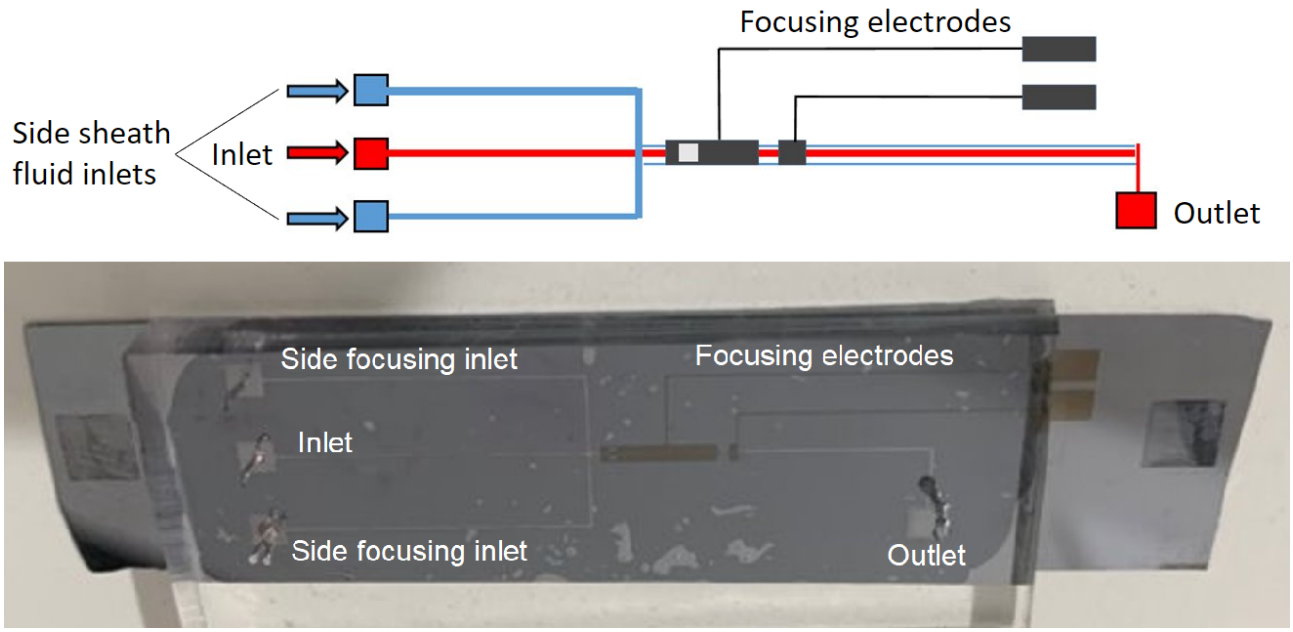

Figure 1: Top) Schematic of flow cytometer, illustrating key components. Fluid flow is visualized with the colored streams, where the red stream is the fluid of interest (dye in the case of the testing experiments), while the blue streams are the focusing sheath fluid (DI water in the case of the testing experiments). Bottom) The produced device, with components annotated just as in the schematic.

Several factors were considered in analysis, with a particular focus on wafer fabrication (since this was the goal of the term project). Energy consumption and material usage directly associated with device construction were completely considered. Additional factors were estimated for analysis purposes, as in [1]. For a full summary of considered factors for our analysis, see Fig. 3 below. Now moving on to the calculations.

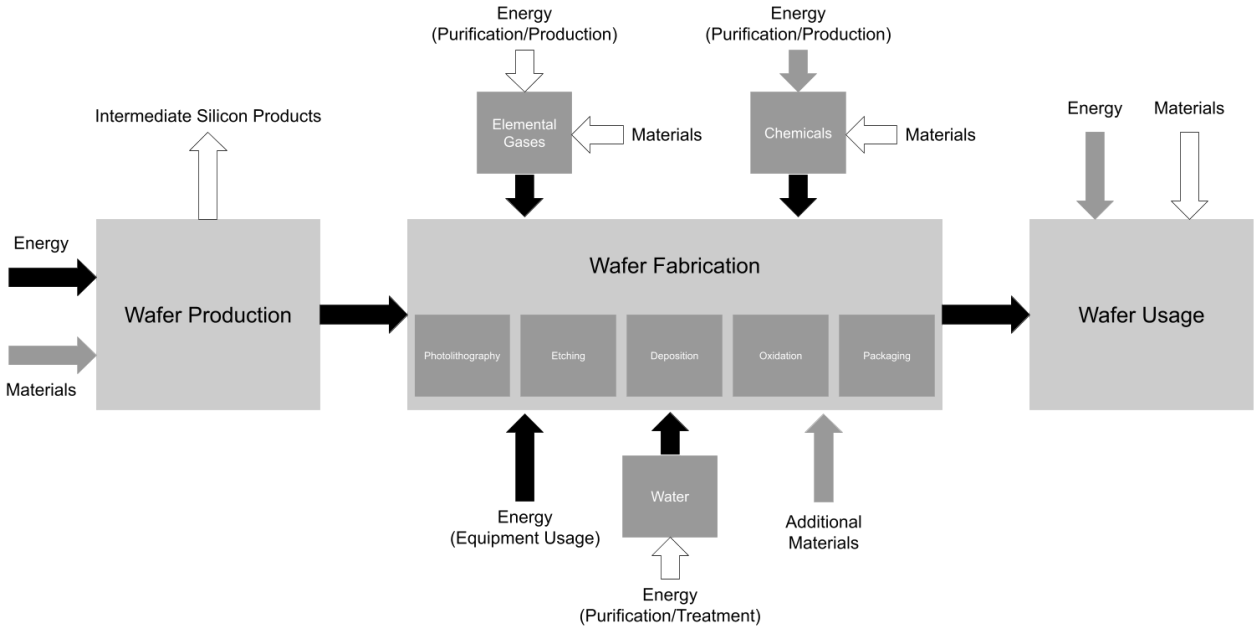

Figure 3: Diagram detailing the factors considered in analysis of the energy/materials consumed for the microfabrication project. White arrows indicate factors that were not considered, gray arrows indicate factors that were partially considered, and black arrows indicate factors that were completely considered. The main considerations were energy usage from equipment in fabrication and material inputs to fabrication (including water, elemental gases, silicon wafer, and chemicals such as etchants and developers). Secondarily, energy usages in producing the inputs and in the use case were partially considered.

Material Consumption

Water was used in several steps of fabrication to rinse off other chemicals and for preparing solutions. Additionally, coolant water was used for the thermal oxidation and evaporation steps. Approximately 3000 mL of water were used for rinsing per major fabrication step, of which there were seven, amounting to approximately 21 L of water per wafer. 425 mL of water were used per BOE etch step (of which there were three) to make etchant solution and 500 mL for the KOH etch, and each of these solutions were used for six wafers. Thus, roughly 300 mL of water were used in solutions per wafer. As for coolant water, the furnace and evaporator consumed roughly 1 gallon (3.8 L) per minute and were used for roughly 60 and 8 minutes, respectively. Six wafers underwent oxidation and deposition at a time, so 43 L of cooling water were used per wafer. Thus, total water consumption per wafer was roughly 64 L. Next, elemental gasses are considered. Nitrogen was used for wafer drying and oxygen for oxidation. Fabrication for 32 wafers used 100 L of nitrogen and 50 L of oxygen, amounting to about 3.1 L of nitrogen and 1.6 L of oxygen per wafer, or converting to grams, in the manner of [1]: 3.6 g N_2 and 2.3 g O_2 per wafer. This is substantially less nitrogen usage than reported in [1] (34.6 kg for the same sized wafer), likely because nitrogen is used as an inert gas in large-scale fabrication processes, while nitrogen was only used for drying in our device project.

Next, chemicals at various stages were considered. For photolithography chemicals, we first consider photoresist. We use the estimate from [1] of 14 g per cm^2 of wafer, of which we estimate 29% is photoresist, given the supplemental data from EIAJ provided in [1]. Additionally, based on the supplemental data from UNEP/UNIDO, the microchip fabrication processes considered in [1] involve two photolithography steps in general, while our process used three. Thus, given the four-inch wafer (surface area of roughly 81 cm^2), we have an estimated 493 g of photoresist used for one wafer. Based on the lab protocols, approximately 100 mL of CD26 developer were used per lithography step, with six wafers using the same developer. This amounts to 50 mL (50 g) of CD26 per wafer [3]. Similar volumes of acetone and isopropyl alcohol were used for two of the lithography steps, amounting to 26 g of each per wafer. However, for the second (aluminum patterning) lithography step, 700 mL of each were used for six wafers, amounting to 92 g per wafer of each. The total for non-photoresist lithography chemicals is thus 286 g per wafer, which is substantially less than the estimate from [1] (1133 g per wafer), likely due to our conservative use of developer. Finally, we consider the etch chemicals. Referring to the lab protocols, each BOE step used 106 mL of HF solution (1.15 g/mL density) and 296 g of NH_4F [4]. There were three BOE steps, and each solution was used for six wafers. Thus, roughly 61 g of HF solution and 148 g of NH_4F were used per wafer. 250 g of KOH were used for bulk substrate etching solution (six wafers per solutions), thus requiring roughly 42 g of KOH per wafer. Finally, 50 mL of PAN etchant (1.58 g/mL density) were used for aluminum etching of six wafers, amounting to roughly 13 g per wafer [5].

Additional materials were used in production, including aluminum for the electrokinetic focusing electrodes and both borosilicate glass and PDMS for packaging. 0.17 g of aluminum were used per wafer during evaporation. Three borosilicate glass slides were used per wafer, amounting to about 13 g per wafer that used glass. 45 g of PDMS monomers and 4.5 g of curing agent were used (this quantity was used for roughly two wafers), and thus roughly 23 g of PDMS and 2.3 g of curing agent were used per wafer that used PDMS. We also consider materials put into wafer production, briefly. The silicon wafer used was a standard, four-inch diameter, 500 μm thickness wafer, weighing about 9.4 g. Roughly 88 g of raw silicon were used in the production of this wafer. Total material use is summarized in Fig. 4.

Energy Consumption

We begin with equipment-related energy usage. Going sequentially, the first lab (photolithography/oxide patterning) used the hotplate for a total of 13.5 minutes, the photoresist spinner for 2 minutes, the mask aligner for 15 seconds, and the profilometer for roughly 5 minutes. Using the provided wattages for these devices, we calculate the energy consumption in joules for the first lithography step to be 0.855 MJ. The second lab (bulk substrate etching) uses the KOH bath heater for 24 minutes, the optical microscope for 5 minutes and the profilometer for 5 minutes, amounting to 0.593 MJ. The third lab (thermal oxidation) uses the furnace for one hour, amounting to 26.1 MJ. The fourth lab (thermal evaporation) uses the evaporator for roughly 7.5 minutes, the photoresist spinner for 1 minute, and the hot plate for 7 minutes. This amounts to 6.888 MJ. The fifth lab (photolithography/aluminum patterning) used the mask aligner for 5 minutes and the hot plate for 2 minutes, amounting to 0.576 MJ. The sixth lab (photolithography/ oxide patterning) used the hot plate for 17 minutes, the photoresist spinner for 1 minute, and the mask aligner for 5 minutes. This amounts to 1.368 MJ. The final lab (anodic bonding/PDMS plasma bonding) used the hotplate for roughly 70 minutes and the anodic bonding apparatus for roughly 60 minutes. PDMS bonding energy was not calculated, as data for the plasma generator device was unavailable. Thus, the final lab used roughly 3.792 MJ. The energy usage for each step is visible graphically in Fig. 5. The total energy used in fabrication was 40.172 MJ. This is substantially less than the estimated energy using data from [1], which would predict around 437 MJ per wafer. Likely this figure is much higher due to increased energy consumption in industrial settings.

For device usage, we estimate energy consumption for fluid flow using reference data for syringe pumps. This gives approximately 9.6 W for one pump [6]. Since each wafer makes three devices with three channels each, this amounts to 86.4 W per wafer. Electrokinetic focusing was not implemented, so energy consumption for this function is not estimated. The estimated usage time based on our testing is approximately 20 minutes, which gives an energy consumption of roughly 0.1 MJ. For wafer production energy consumption, we adopt data from [1]. The electricity consumption to produce one square cm of wafer calculated in [1] is roughly 0.34 kWh, or 1.224 MJ, which amounts to about 99.1 MJ for our wafer. We also partially estimate energy used in chemical production using data from [1], which suggest 1.45 MJ per square centimeter of wafer, or

around 117 MJ per wafer. The estimates for energy consumption from [1] are notably higher than calculated values from our laboratory processes. These could also be attributed to substantial improvements in technology, since [1] reflects the state of the semiconductor industry in 2002. Twenty years seems to make quite a difference in energy consumption for semiconductor manufacturing.

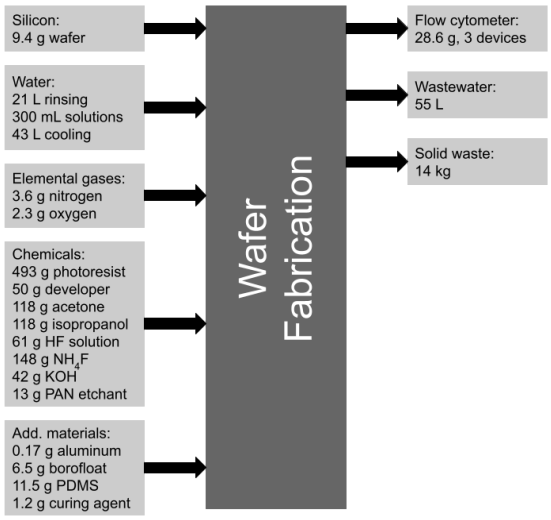

Figure 4: Diagram showing inputs and outputs in wafer fabrication. The calculation process is summarized in the Materials Consumption section above. For clarification, the amounts for PDMS, curing agent, and borofloat are given as half of what would be required for one wafer, since half of the wafers were packaged with PDMS and half with borofloat. Additionally, each wafer produces three flow cytometer devices, so an individual flow cytometer would be 9.5 g on average. For outputs, we assume the same ratio of wastewater to input water, and the same ratio of solid waste to input as [1]. The given solid waste figure seems very large, but this encompasses all disposed chemicals, cleaning materials such as paper towels, etc. Still, the number is likely an overestimate, since it reflects trends in industrial production from two decades ago.

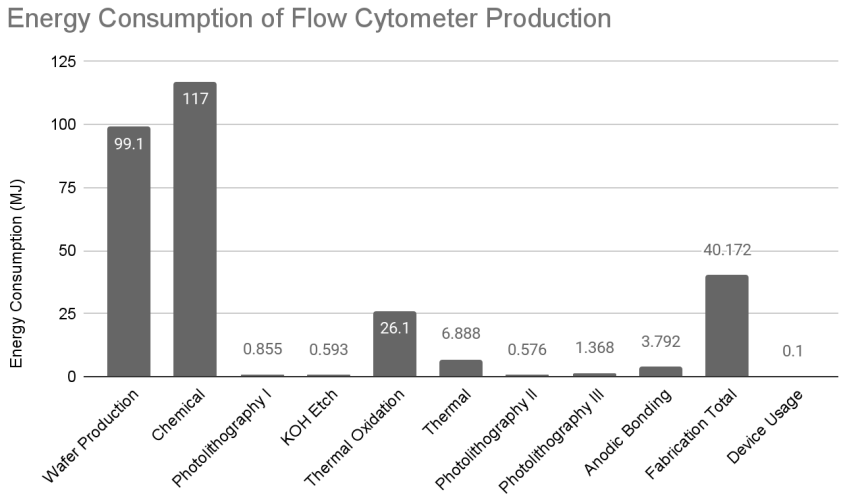

Figure 5: Energy consumption of various steps of our fabrication project. Data for wafer and chemical production (pre-fabrication steps) was sourced from [1]. These values are much higher than our calculated values, likely owing to advances in semiconductor manufacturing technology over the past two decades.

References:

[1] E. D. Williams, R. U. Ayres, and M. Heller, "The 1.7 kilogram microchip: energy and material use in the production of semiconductor devices," *Environmental Science & Technology*, vol. 36, no. 24, pp. 5504–5510, 2002

[2] L. Zong, B. Zhu, Z. Lu, Y. Tan, Y. Jin, N. Liu, Y. Hu, S. Gu, J. Zhu, and Y. Cui, "Nanopurification of silicon from 84% to 99.999% purity with a simple and scalable process," *Proceedings of the National Academy of Sciences*, vol. 112, no. 44, pp. 13473–13477, 2015.

[3] *Microposit - MF - CD26 Developer*; Dow Chemical Company; Marlborough, MA; 08/20/2012

[4] *Hydrofluoric Acid*; Sigma Aldritch; St. Louis, MO; 12/15/2021

[5] *Aluminum Etchant Type A*; Sigma Aldritch; St. Louis, MO; 10/02/2021

[6] *NE-1000 Syringe Pump - User Manual*; New Era Pump Systems Inc.; Farmingdale, NY; 04/06/16

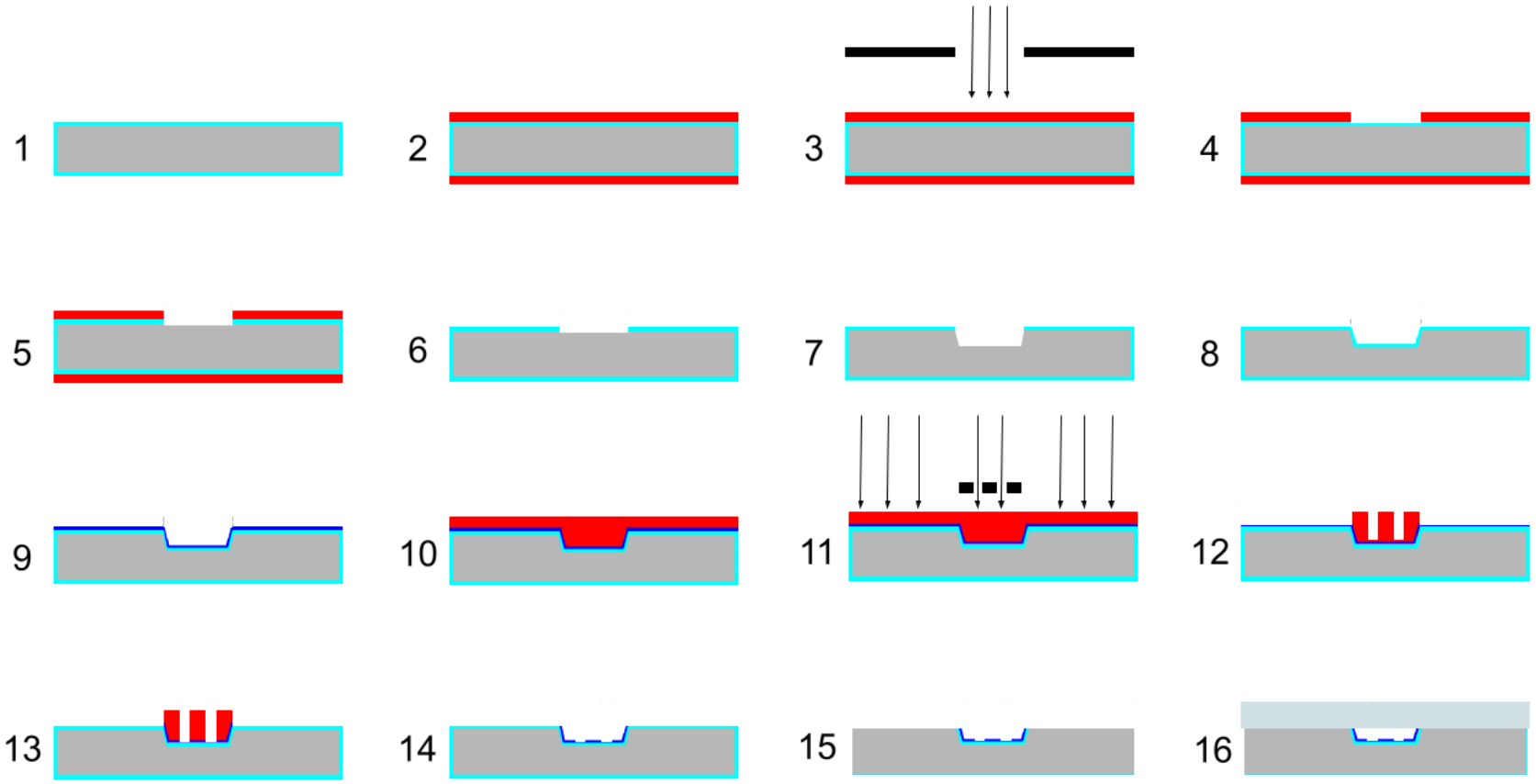

Figure 2: Process diagram of flow cytometer construction. Legend: dark gray (silicon), cyan (oxide), red (photoresist), black (photomask), black arrows (UV radiation), blue (aluminum), light gray (packaging material, either PDMS or borosilicate glass). 1) The starting, pre-oxidized silicon wafer. 2) Photoresist added for microchannel patterning. 3) UV exposure step with aligned mask for microchannel patterning. 4) Patterned photoresist after development. 5) Buffered oxide etch (BOE) step to create channel pattern in oxide. 6) Photoresist removal with acetone and isopropyl alcohol (IPA). 7) Bulk substrate etching of silicon with KOH to form microchannels. 8) Thermal oxidation to reform oxide on microchannels, electrically isolating silicon substrate. 9) Aluminum deposition by thermal evaporation for electrode construction. 10) Photoresist added for next photolithography step. 11) UV exposure step with aligned mask for electrode patterning. 12) Patterned photoresist after development. 13) Aluminum etched with PAN to form electrodes. 14) Photoresist removed with acetone and IPA. 15) BOE to remove oxide (photolithography step to protect aluminum not shown). 16) Packaging with either anodic bonding or PDMS plasma bonding.